Experimental Demonstration of Gain Cells with Self-Aligned Oxide Transistors for Reduced Capacitive Coupling

Jay Sonawane, Sunbin Deng, Faaiq Waqar, Omkar S Phadke, Chengyang Zhang, Ming-Yen Lee, Suman Datta, Shimeng Yu*

Georgia Institute of Technology, U.S.A

This work presents a comparative experimental study on parasitic effects in gain-cell (GC) memories using overlapped (OL) and self-aligned (SA) amorphous oxide semiconductor (AOS) transistors. Both OL and SA transistors are used as testbeds and evaluated for their impact on 2T0C [1] and 3T0C [2] GC configurations. Our results demonstrate that SA-based 3T0C GCs significantly reduce parasitic capacitance, eliminating storage node voltage drop (ΔV_{SN}), and achieving 10× retention over the OL counterparts.

Fig. 1 shows (a) the OL, SA transistors' schematic, and 2T0C, 3T0C circuit diagrams. In Fig. 1 (b), the experimental transfer characteristics and $C_{GD} + C_{GS}$ vs V_{GS} curves of SA and OL AOS transistors are compared. The measured off-state $C_{GD} + C_{GS}$ of the SA transistors is below the noise floor of the measurement setup, indicating that off-state parasitic capacitance of SA transistors decreases more than 265× compared to that of the OL transistors.

The gain cell designs are tested experimentally using voltage sense and current sense-based methods (Fig. 1 c). The difference between VS and CS is that the write '1' is for OFF and ON state of read transistor respectively. It is demonstrated that for SA 2TG0C GC, the capacitive coupling between WWL and SN is reduced for CS scheme. The WWL-to-SN capacitance coupling is significantly suppressed with >96% ΔV_{SN} reduction, transitioning from OL to SA 2T0C GC (Fig. 2 a). Also, in SA 2T0C GC, VS shows no sense margin between Write '1' and '0'. This is attributed to the reduced C_{OFF} in the case of SA transistors.

For the 3T0C GC, the effect of coupling reduction is observed to be consistent with the 2T counterpart (Fig. 2 b). For SA 3T0C GC, the effect of $C_{WWL\text{-}SN}$ is diminished, and no capacitive coupling is observed experimentally, indicating that $\Delta V_{SN} = 0$ V. Thus, the SA geometry helps in retaining the sense margin completely in 3T0C GC.

The retention time improvement is found to be 10× in SA geometry, compared to overlapped GC in both 2T and 3T 0C GC (Fig. 2 c). Further, a stable read at high-speed write is observed for SA 2T0C GC. These findings highlight the advantages of SA structure in enabling high-performance, parasitic-aware GC design.

References

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* Corresponding author: shimeng@ece.gatech.edu

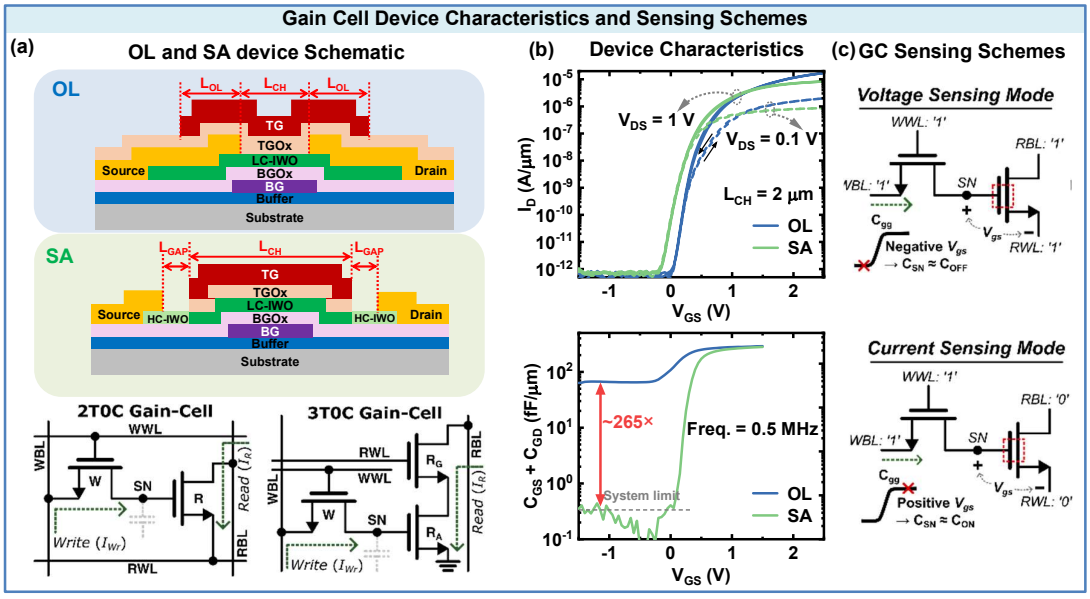

Fig. 1: (a) Schematic of OL and SA transistor and circuit diagram of 2T0C and 3T0C GC. (b) Comparison of transfer characteristics, and C_{GD} + C_{GS} vs V_{GS} curves of SA and OL AOS transistors. (c) Illustration of voltage and current sensing schemes used in this study.

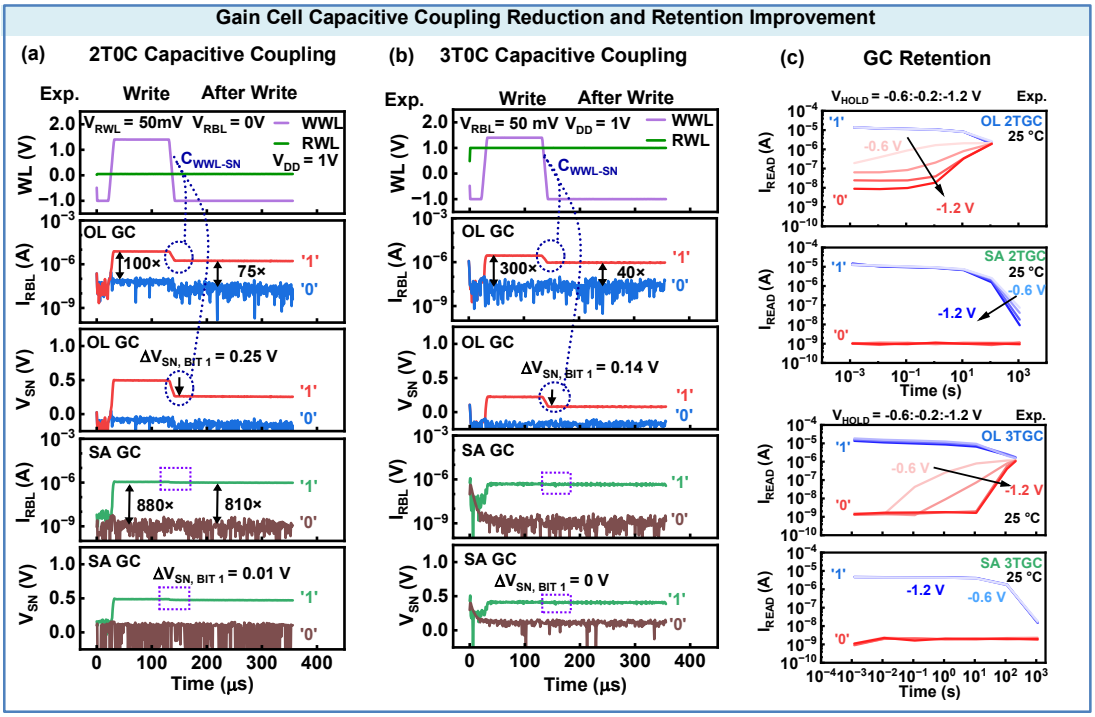

Fig. 2: Demonstration of capacitive coupling reduction in SA GC for (a) 2T0C and (b) 3T0C (c) Experimental retention test for 2T0C and 3T0C GC show 10× improvement in SA GC.